UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,276	08/27/2003	Shinya Watanabe	Q76956	4435

23373 7590 08/05/2005

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
DOLAN, JENNIFER M	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,276	WATANABE ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/6/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 28, 29, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,926,586 to Dragone et al. in view of Japanese Patent Publication No. 05-333222 to Oguchi et al. (cited by applicant).

Regarding claim 28, Dragone discloses a chip manufacturing method, comprising: forming a plurality of elements on a wafer (figure 5), and cutting out a plurality of chips, each chip including one element (column 2, lines 50-57; column 4, lines 1-16), wherein each element includes a substantially arcuate shape (curved boundaries in central/dotted-line region of figure 5); each chip includes a concave boundary line and a convex boundary line that substantially

follow an outline of one of the elements (column 4, lines 4-13), and the concave boundary line of one chip is shaped the same as the convex boundary line of another chip (column 4, lines 4-13; figure 5; if the chips are separated using a nonlinear cut substantially following the contour line of the elements, then it is apparent that the same cut forms the concave boundary of the upper chip and the convex boundary of the lower chip in figure 5).

Dragone fails to explicitly disclose more than one line of elements, but rather only depicts a single line (figure 5).

Oguchi teaches that it is common and expected in the art of optical elements to form them in a plurality of lines (see figure 2), with each line containing a plurality of elements, such that substantially the entire wafer is filled with optical chip elements (see figure 2). Oguchi further teaches that first the wafer is separated into lines, and then each line is separated into individual chip elements (see paragraph 0014).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the optical element of Dragone may be formed in more than one line, as suggested by Oguchi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide the device in more than one line, because it is common and well known in the art of device fabrication to tile devices across the entire usable space of a wafer, in order to increase the number of devices yielded per wafer, as is appreciated by a person having ordinary skill in the art (also see figure 2 of Oguchi et al). Since there appears to be no specific material change, unexpected result, or specific advantage resulting from providing the second line of devices, other than the fact that more devices are provided on the wafer, and since the concept of providing as many 'lines' of devices that may fit on a wafer is well established in

the art of semiconductor device manufacturing, it is the Examiner's opinion that the addition of a second line of devices to the invention of Dragone constitutes a mere duplication of parts – a modification held by the Court as having no patentable significance. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

Regarding claim 29, Dragone discloses that the chips are cut using a laser beam (column 4, lines 18-25).

Regarding claim 32, Dragone discloses that dicing is used to cut the straight-line portions of the contours (column 4, lines 18-25; only the curved portions are cut with the laser; also see column 2, lines 5-26).

Regarding claim 33, Dragone discloses that a plate is mounted on at least a portion of the chip (column 5, lines 10-15).

4. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dragone et al. in view of Oguchi, as applied to claim 28, supra, and further in view of U.S. Patent No. 5,776,796 to Distefano et al.

Dragone fails to teach that ultrasonic vibration or hydraulic pressure can be used to cut the chips from the wafer.

Distefano teaches that laser cutting, ultrasonic vibration, and hydraulic pressure cutting are all well-known and interchangeable means for dicing a chip component (see column 5, lines 19-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the method of Dragone as modified by Oguchi uses ultrasonic vibration

or hydraulic pressure for cutting the chips from the wafer, as suggested by Distefano. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use ultrasonic vibration or hydraulic pressure cutting, because Dragone shows that even non-ideal dicing means, such as lasers, are appropriate to use with the methods taught by Dragone (see Dragone, column 4, lines 5-35). Since Distefano teaches that all of a laser, ultrasonic vibrator, or hydraulic jet are well known and recognized equivalent means for dicing a semiconductor wafer, a person skilled in the art could apply any of these to the methods taught by Distefano with a reasonable expectation of success.

5. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dragone in view of Oguchi and U.S. Patent No. 5,745,631 to Reinker.

Dragone discloses forming a plurality of elements on a wafer (figure 5); cutting out a plurality of first and second chips, each chip having an optical multiplexer element (see column 1, lines 5-10), where the first and second chips have substantially similar contours having a (figure 5; the "first chip" can be taken as the 'highest chip' and "the second chip" as 'the second-highest chip'), wherein each element includes a substantially arcuate shape (curved boundaries in central/dotted-line region of figure 5); each chip includes a concave boundary line and a convex boundary line that substantially follow an outline of one of the elements (column 4, lines 4-13), and the concave boundary line of one chip is shaped the same as the convex boundary line of another chip (column 4, lines 4-13; figure 5; if the chips are separated using a nonlinear cut substantially following the contour line of the elements, then it is apparent that the same cut

forms the concave boundary of the upper chip and the convex boundary of the lower chip in figure 5).

Dragone does not teach bonding the chips together using an adhesive and arranging the elements in two or more lines on the wafer.

Reinker discloses an optical multiplexer formed by stacking chips and flowing an adhesive (column 1, lines 25-45; column 2, lines 1-30; figures 9-11).

Oguchi teaches that it is common and expected in the art of optical elements to form them in a plurality of lines (see figure 2), with each line containing a plurality of elements, such that substantially the entire wafer is filled with optical chip elements (see figure 2). Oguchi further teaches that first the wafer is separated into lines, and then each line is separated into individual chip elements (see paragraph 0014).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Dragone, such that the chips are stacked, as suggested by Reinker, and such that multiple lines of elements are formed on the wafer, as suggested by Oguchi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to stack the chips, because doing so allows for the formation of larger scale OEICs, such that a greater number of wavelengths can be accommodated by a multiplexer (see Reinker, column 1, lines 5-30; column 2, lines 25-30; column 5, lines 45-65). A person having ordinary skill in the art would have further been motivated to provide the device in more than one line, because it is common and well known in the art of device fabrication to tile devices across the entire usable space of a wafer, in order to increase the number of devices yielded per wafer, as is appreciated by a person having ordinary skill in the art (also see figure 2 of Oguchi et al). Since

there appears to be no specific material change, unexpected result, or specific advantage resulting from providing the second line of devices, other than the fact that more devices are provided on the wafer, and since the concept of providing as many 'lines' of devices that may fit on a wafer is well established in the art of semiconductor device manufacturing, it is the Examiner's opinion that the addition of a second line of devices to the invention of Dragone constitutes a mere duplication of parts – a modification held by the Court as having no patentable significance. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

6. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dragone et al. in view of Oguchi and Reinker as applied to claim 34 above, and further in view of U.S. Patent No. 6,379,909 to Forbes et al.

Dragone fails to suggest that the first chip is cut from a first wafer, and the second chip is cut from a second wafer.

Forbes teaches a stacked chip structure in which the chips can alternately be cut from the same wafer or from different wafers (column 1, lines 20-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Dragone as modified by Reinker, such that the chips are cut from different substrates, as suggested by Forbes. The rationale is as follows: A person having ordinary skill in the art would have been motivated to cut the chips from different substrates, because bonding chips cut from different substrates is well-known in the art, and provides the advantages of allowing each device to be fabricated according to its individual performance needs or fabrication processes, as is appreciated by one skilled in the art (see Forbes, column 1,

lines 25-60). Since the invention of Dragone as modified by Reinker includes lasers operating at different wavelengths, and accompanying waveguides appropriate to such wavelengths (see Reinker, column 1, lines 5-30, column 2, lines 25-30, column 5, lines 45-65), it would be expected by a person having ordinary skill in the art that the waveguides and lasers from each layer of the array should be formed on different substrates, such that the individual emission properties can be optimized.

Response to Arguments

7. Applicant's arguments with respect to claims 28-36 have been considered but are moot in view of the new grounds of rejection.

Insofar as the arguments pertain to the presently applied rejection, the Examiner would like to address the issue raised on page 5 of the Applicant's remarks, pertaining to the rejection of claims 28, 29, 32, and 33 over Dragone:

The Applicant suggests that one of the advantages of the presently claimed subject matter is that optical characteristic tests may be performed prior to cutting along the curved paths. The Examiner respectfully points out that the claims do not include a limitation of conducting an optical characteristic test prior to cutting along the curved paths. Furthermore, the newly added limitation of providing the devices in more than one line does not affect or enable such an optical characteristic test, since the devices are first cut into lines, and hence will be substantially identical to the single line taught by Dragone, before an optical characteristic test or a separation into individual chip elements is conducted.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,596,185 to Lin et al. discloses separating adjacent optical components using a curved cutting line.

U.S. Patent No. 6,021,267 to Bonn et al. and U.S. Patent No. 5,341,024 to Rosotker disclose methods for efficiently packing chip elements on a wafer in order to maximize yield.

U.S. Patent No. 6,535,670 to Takei et al. discloses forming an optical element in two lines of devices, separating the two lines, and then separating individual chip elements from each line.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

LAURA M. SCHILLINGER
PRIMARY EXAMINER